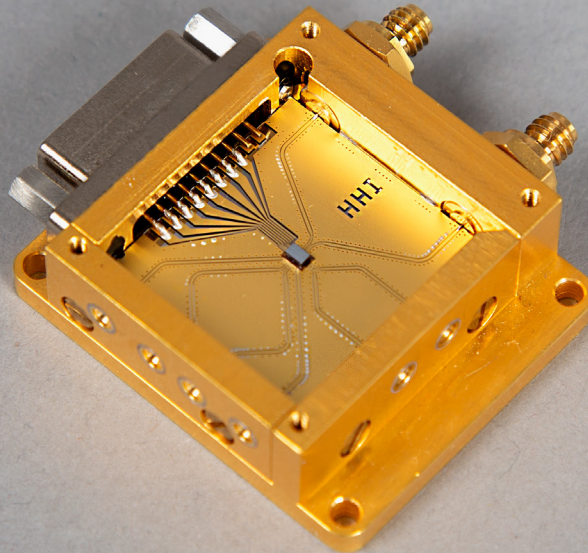


HIGH-SPEED 2:1 ANALOG MULTIPLEXER MODULE



AT A GLANCE

High-speed 2:1 analog multiplexer (AMUX) module for interleaving two digital-to-analog converters (DACs)

Features

- 2:1 AMUX SiGe IC in gold-plated housing
- 2 differential G3PO data inputs, 1 differential G3PO clock input, 1 differential 1mm data output
- 6-dB data path bandwidth: 61 GHz
- 6-dB clock path bandwidth: 55 GHz
- 1 V_{pp} differential input voltage

Applications

- Arbitrary Waveform Generators (AWG)
- Other high-speed measurement systems
- Evaluation of DAC interleaving for next generation high-speed DACs

Technical Background

In ultra-broadband optical transmission systems, the limited analog bandwidth of both electrical and opto-electrical components is still a bottleneck. Especially, the analog bandwidth of cost- and energy-efficient data converters in complementary metal oxide semiconductor (CMOS) technology cannot be increased substantially with new CMOS technology nodes. For digital-to-analog converters (DACs), interleaving is a promising way forward to generate electrical signals with greater analog bandwidth by combining the output of multiple DACs. Especially interleaved DACs using analog multiplexers (AMUX) allow a substantial increase of both the analog bandwidth and the sampling rate. AMUX-DACs are therefore promising candidates for next generation high-speed DACs used in measurement equipment and integrated optical transceivers.

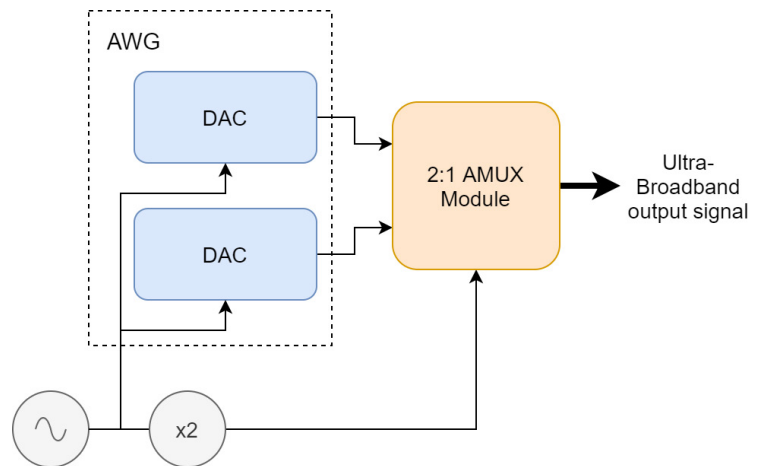


Figure 1: Application example for the 2:1 AMUX module with two DACs: The DAC output signals are combined by the AMUX to form an ultra-broadband output signal, which has twice the sampling rate and bandwidth. A common clock source drives both DACs and the AMUX.

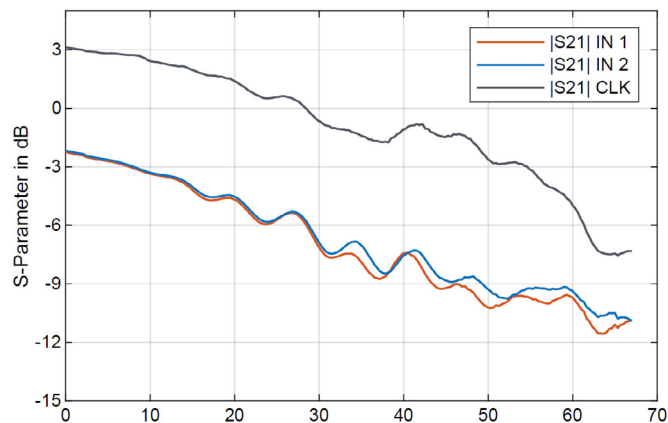


Figure 2: Clock and data path frequency responses of the AMUX module

Jonathan Schostak
Photonic Networks and Systems

Phone +49 30 31002 414
products-pn@hhi.fraunhofer.de

Fraunhofer Heinrich Hertz Institute
Einsteinufer 37, 10587 Berlin
Germany

www.hhi.fraunhofer.de/pn

Additional Features

- Half-clock input (with respect to output sampling frequency)
- Fully differential design
- 6 optional control voltages and currents with 10-pin Micro-D connector