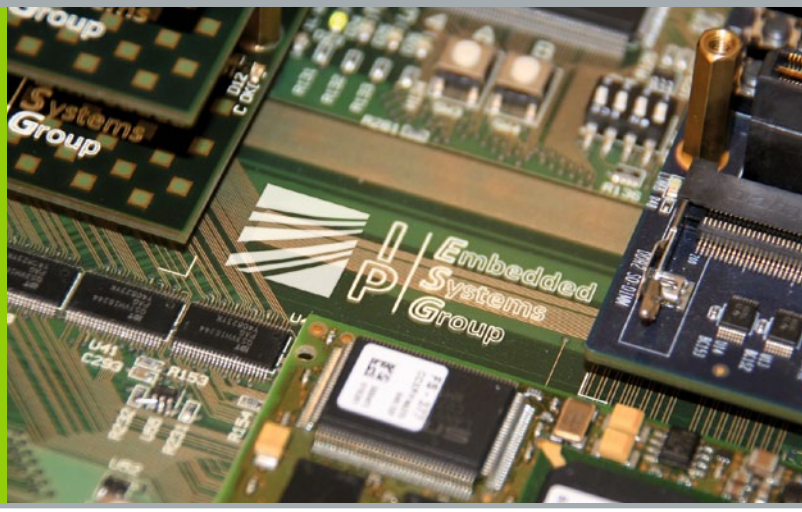
Fraunhofer
Heinrich Hertz Institute

Enhanced Low Latency Video Codec

An H.264/AVC Video Codec IP with outstanding low latency



The Fraunhofer Heinrich Hertz Institute HHI offers a range of H.264/AVC compliant codecs (IPs) for use in industrial applications. Specially tailored to real-time applications, the IPs allow coding of up to 1080p resolution on current FPGA technologies. The codecs are fully hardwired implementations with low power consumption and minimal resource usage.

Challenges

Many applications for live video encoding require low latency like Advanced Driver Assistance Systems or visual medical surgery equipment which is highly dependent on video data real-time processing. The Enhanced Low Latency Video Codec (ELLVC) allows coding of intra and inter-frames to combine low latency demands with efficient video compression features.

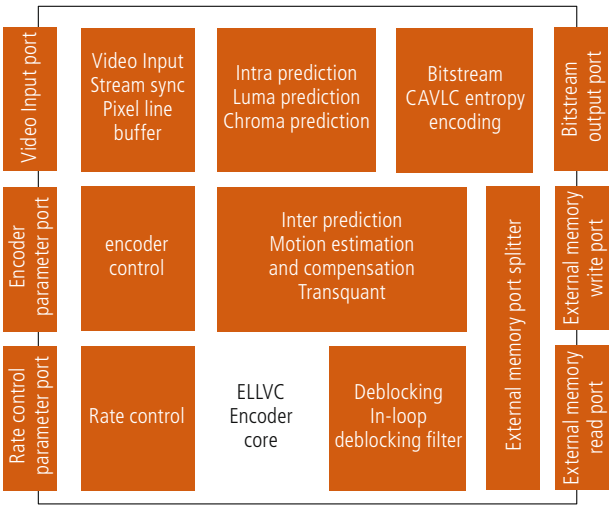
Technical Background

To avoid the typical bitrate peaks often arising in Intra/ Inter coding, a special "Intra refresh" mode has been implemented. The ELLVC IP has low requirements for on-chip and off-chip memories. The type of external memory does not matter as long as the read and write accesses are fast enough to satisfy the real-time requirements of the codec. The external memory interface of the IP is very flexible and can be connected to memory controllers already available on the market.

Because processing of one macroblock needs only around 600 clock cycles to complete, the IP has very low clock demands.

The ELLVC IP is ready to be integrated into larger systems through flexible interfaces that can be adapted to specific needs, if necessary.

The codec is available as VHDL description synthesizable for FPGA and ASIC Technolgies. Existing testbenches and C reference models allow the hardware designer to simulate the ELLVC IP core using state of the art simulation environments.



ELLVC IP block diagram

Videoformat	Sample rate (MHz)	Lines	Active lines	Samples per line	Active samples per line	width_in_mbs	height_in_mbs	F_{min} (MHz)
576i50[2]	27[2]	625	576	864	720	45	36	24.7
480i60[1]	27[2]	525	480	858	720	45	30	24.7
720p50 720p60	74.25 74.25	750 750	720 720	1980 1650	1280 1280	80 80	45 45	109.8 131.8
1080p25	74.25	1125	1080	2640	1920	120	68[3]	124.4
1080p30	74.25	1125	1080	2200	1920	120	68[3]	149.3

Overview of common HD/SD resolutions and needed clock cycles

Benefits

- H.264/AVC baseline profile compliant
- Intra refresh feature to avoid bitrate peaks
- Inter prediction supports all macroblock partition sizes
- Low latency below 2 frames
- SD and full HD resolutions up to 1080p with 30fps supported
- Low clock demands for real-time coding
- Low resource demands (Numbers for Xilinx Virtex-6 FPGA LX240T)
  - Slices: 34.000
  - Slice registers: 90.000
  - Slice LUTs: 98.000
  - Block Ram: 212
  - DSP48E1s: 65

Future Objectives

Fraunhofer HHI offers both encoder and decoder solutions. The encoder solution is already available. The decoder solution is expected to be released in Q2/2012.

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