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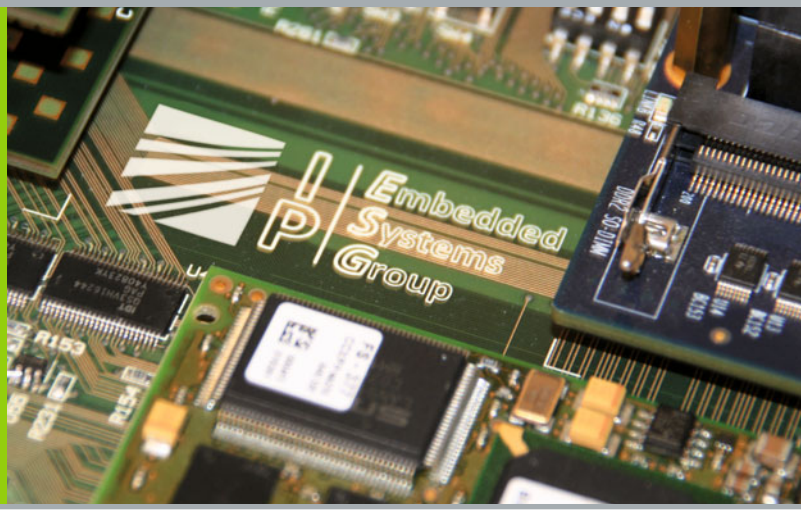
Ultra Low Latency Video Codec

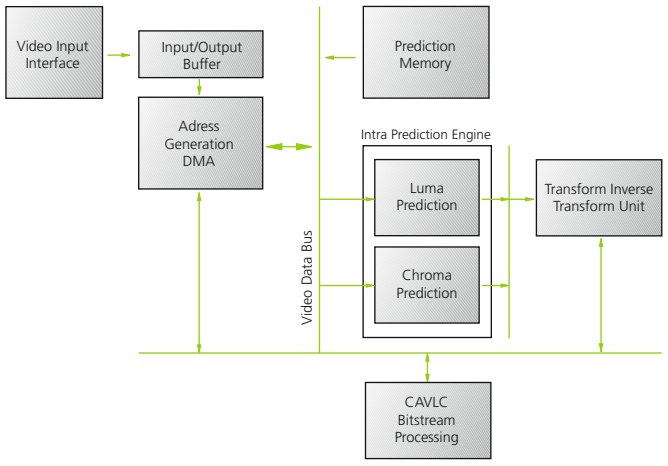
An H.264/AVC based Video Encoder with Low Memory Requirements for Real-Time Applications



The Fraunhofer Heinrich Hertz Institute HHI offers an ultra-low latency video encoder compliant with the H.264 baseline profile. The encoder is implemented as a hardwired solution that can be mapped on FPGAs or ASICs without any need for external memory. Specially tailored to real-time applications, it allows for up to 1080p encoding with today's FPGA or ASIC technologies.

Challenges

Many applications for live video encoding require low latency like Advanced Driver Assistance Systems (ADAS) or visual medical surgery equipment which are highly dependent on video data real-time processing. Today's advanced video standards such as H.264/AVC might offer a huge range of coding features, but many of these features still depend on temporal or spatial neighbors – which leads to latency during the encoding process. Low-latency encoding thus requires a smart choice of the encoding features to be applied.



Block Diagram of the Ultra Low Latency Encoder

Technical Background

Fraunhofer HHI analyzed the efficiency of different H.264 encoding methods and selected the most efficient and low-latency compliant features. The resulting encoder uses intra-prediction modes and content-adaptive VLC.

The latency between input and output frames is below one macroblock line. The quality of the encoded data stream is comparable to the H.264 reference encoder when using similar encoding features.

Besides low latency, the chosen encoding features also lead to very low memory requirements, e.g. for PAL resolution, only 20kByte of on-chip memory and no off-chip memory at all is needed. The encoder is a fully hardwired implementation and requires only 170k gates (UMC 0.18µm process). Interfaces to common SOC busses such as AXI AHB allow easy integration with other system components.

The encoder is available in VHDL description and runs successfully in real-time on an Altera StratixIII-based FPGA (Fraunhofer HHI HEP II evaluation board). An executable reference model in C as well as testbenches for system level and block level verification can also be provided.

A symetrical implemented decoder is also available with similar contraints in terms of clock frequency and complecity.

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Benefits

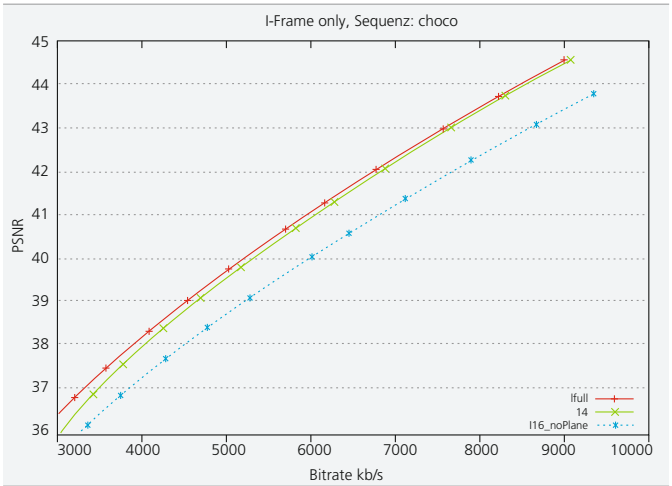
- Low delay, low latency codec delay < 1 macroblock line (at least 3ms)
- H.264 baseline profile subset
- Coding of progressive video using H.264 Main Profile syntax with Baseline toolset (no CABAC used)
- Coding and decoding using all 4×4 intra coded blocks with prediction modes and 16×16 modes
- Coded stream can be decoded with every H.264 compliant decoder e.g. DVD Player with H.264 support
- Picture resolution up to HD
- YUV 4:2:0 8Bit
- Data rates up to 60Mbit/s
- clock cycle requirements

  640x480@25Hz => 18 MHz

  800x600@30Hz => 33,75 MHz

  1280x720@60Hz => 129 MHz

  1920x1080@30Hz => 145,8 MHz



Encoder Quality Comparison

References

Successor versions of the current encoder will support processing of 10bit 4:2:0 video data and Scalable Video Coding (SVC, available Q3/2011) with similar clock cycle requirements to the current version. Additionally a hardwired decoder solution is available.

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